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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,416	04/07/2005	Hong Goo Choi	P27698	4900

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/530,416	CHOI ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of claims 1-9 in the reply filed on January 23, 3006 is acknowledged. The traversal is on the ground(s) that in determining unity of invention the invention will be considered to have unity if claims are drawn to "a product and a process specially adapted for the manufacture of said product". Examiner finds the grounds persuasive and the restriction improper, therefore all claims will be examined.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant describes the advantages of the use of quantum channels in a photodetectors MOSFET in the specification, however applicant does not clearly describe the intended meaning of quantum channels. Quantum wells are known in the art of photodetectors, however it is unclear if applicant is referring to a quantum well channel or another type of quantum channel.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Regarding claims 1 and 10, it is unclear what applicant means by having a SOI wafer "activated".

6. Regarding claim 11, applicant recites the limitation "forming an additional gate" in line 3. However, applicant has never discloses an original gate. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-10 and 14-16 are rejected under 35 U.S.C. 103(s) as being anticipated by U.S. Pat. No. 6,784,466 to Chu et al. in view of U.S. Pat. No. 6,091,076 to Deleonibus.

9. Regarding claim 1 and 10, as far as the claims can be understood, Chu et al. discloses a photodetector using a MOSFET with a quantum channel (Figure 13 element 140), a quantum channel (Fig 13 element 122 and column 10 lines 66-67 and column 11 line 1) formed on the center of a wafer activated, a gate oxide film (127) covering the quantum channel, a source (130) and a drain (130) formed at both ends of said channel area; and metal layers (138) connected with the source and the drain.

Chu et al. lacks teaching the use of an SOI wafer. Deleonibus teaches the use of a SOI wafer for a quantum channel MOSFET (Fig 8, column 8, lines 19-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chu et al. to use a substrate of SOI in order to reduce leakage and capacitance.

10. Regarding claim 2, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, further comprising a gate (128) formed additionally on said gate oxide film so as to control carrier current in said quantum channel, said gate being connected to the metal layers.

11. Regarding claim 3, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, wherein said gate oxide film comprises oxides including SiO_2 (column11 line 9)

12. Regarding claim 4, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, wherein said MOSFET comprises N-P-N type MOSFET (Figure 13 element 140).

13. Regarding claim 5, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, wherein said MOSFET comprises P-N-P type MOSFET (Figure 13 element 139).

14. Regarding claims 6 and 7, Chu et al. as modified discloses the method of claim 1 as described above. Chu et al. as lacks teaching the gate oxide film having a depth of 1nm ~ 50nm and the source and drain having a depth of less than 1000nm. Deleonibus teaches the depth of the source and drain as 8nm (column 7 lines 21-25), which is less

than 1000nm. Deleonibus does not disclose the depth of the gate oxide film, however, based on the relative depth of the gate oxide to the depth to the source and drain of 8nm, it would be reasonable for one skilled in the art to find the gate oxide film to have a depth about half the depth of the source drain, 4nm, which is within the range of 1nm ~ 50 nm. Further, the depths of the source, drain, and gate oxide films are viewed as nothing more than obvious design variations of that could be easily ascertained through routine experimentation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chu et al. to use the depth of the gate oxide film to be between 1nm ~ 50nm and the depth of the source and drain as less than 1000nm in order to maximize the performance of the device.

15. Regarding claim 8, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, wherein said metal layers connected with said source and said drain comprise a metal selected from the group consisting of Al, Ti, W, In, Co, Au, Ni and Cr (column 8 lines 26-29).

16. Regarding claim 9, as far as the claim can be understood, Chu et al. as modified discloses the photodetector of claim 1, wherein said metal layers connected with said source and said drain comprise a metal compound including a metal selected from the group consisting of Al, Ti, W, In, Co, Au, Ni and Cr (column 8 lines 26-29).

17. Regarding claim 14, as far as the claim can be understood, Chu et al. as modified discloses the method as described by claim 10, wherein the number of quantum channels formed is one or more (Figure 13 shows a quantum channels 122 and 124).

18. Regarding claims 15 and 16, Chu et al. as modified discloses the method of claim 10 as described above. Chu et al. as lacks teaching the gate oxide film having a depth of 1nm ~ 50nm and the source and drain having a depth of less than 1000nm. Deleonibus teaches the depth of the source and drain as 8nm (column 7 lines 21-25), which is less than 1000nm. Deleonibus does not disclose the depth of the gate oxide film, however, based on the relative depth of the gate oxide to the depth to the source and drain of 8nm, it would be reasonable for one skilled in the art to find the gate oxide film to have a depth about half the depth of the source drain, 4nm, which is within the range of 1nm ~ 50 nm. Further, the depths of the source, drain, and gate oxide films are viewed as nothing more than obvious design variations of that could be easily ascertained through routine experimentation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chu et al. to use the depth of the gate oxide film to be between 1nm ~ 50nm and the depth of the source and drain as less than 1000nm in order to maximize the performance of the device.

19. Claims 11-13 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,784,466 to Chu et al. in view of U.S. Pat. No. 6,091,076 to Deleonibus as applied to claim 10 above, and further in view of U.S. Pat. No. 6,998,641 to Makita et al.

20. Regarding claim 11, as far as the claim can be understood, Chu et al. as modified discloses method as defined by claim 10. Chu et al. further discloses forming a gate (128) on the gate oxide film (127). and depositing metal layers after forming contacts (135) on the gate. Chu et al. lacks teaching using forming the gate by means of

lithography. Makita et al. teaches forming a gate by means of lithography in Figure 10A, elements 617-620 are gates, column 24 lines 16-18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Chu et al. use lithography to form the gates as in Makita et al. because lithography is one of the best methods currently in use for manufacturing small scales devices.

21. Regarding claim 12, as far as the claim can be understood, Chu et al. as modified discloses the method as defined by claim 10. Chu et al. al lacks teaching the step of forming an activated area is carried out by means of activated area mask, photolithography process, and etching process. Makita et al. teaches forming an activated area is carried out by means of activated area mask (611-616), photolithography process, and etching process (column 24 lines 29-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Chu et al. use an activated area mask, photolithography process, and etching process to form the activated area as in Makita et al. because masks, photolithography, and etching are well known methods currently in use for manufacturing small scales devices.

22. Regarding claim 13, as far as the claim can be understood, Chu et al. as modified discloses the method as defined by claim 10. Chu et al. al lacks teaching the step of forming a quantum channel is carried out by means of lithography technology including an etching process using a photomask. Makita et al. teaches forming a channel is carried out by means of lithography technology including an etching process using a photomask (column 23 lines 55-58). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to further modify Chu et al. use for the quantum channels using a lithography technology including an etching process using a photomask as in Makita et al. because lithography, etching and photomasks are well known methods currently in use for manufacturing small scales devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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